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The Control Circuit Design of Radar Data Acquisition System

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Abstract: Control circuit is a key part of the radar data acquisition system. Control circuit mainly includes the data acquisition timing and system logic relation and interface circuit timing, FPGA and CPLD chip is used to design the control circuit of dual channel radar data acquisition system. In this paper, design of the plus interface timing circuit and Multi-objective continuous tracking and collecting system control circuit is completed. The acquisition system has solved the real-time performance of the radar target data acquisition from the hardware, it overcomes the phenomenon that the target information is lost in the traditional radar target data acquisition, it has strong universality.

Keywords: Control circuit design, interface timing circuit design, radar data acquisition system, the FPGA and CPLD.

1. INTRODUCTION

Radar target recognition [1] is based on target echo signal in radar system detection background, through the signal and information processing methods, such as data acquisition and preprocessing, feature extraction, matching and classification, automatically identifying unknown target categories and attributes. The rradar data acquisition system is a key part of the radar target recognition system.

2. COLLECTION SYSTEM COMPONENTS AND FEATURES

2.1. Collection System Composition

Fig. (**1**) shows the principle component diagram of the dual channel radar data acquisition system, the system is composed of two channels analog input part, 12 bit A/D converter, multilevel data buffer, large capacity data memory, system logic control circuit and detection board interface circuit.

In the acquisition board, I, Q two analog signals after 12 bit high speed A/D conversion, and then the data is locked into a multi-level data buffer. The high 8 bits of the I channel or the Q channel can enter the detection board, and the detection results are passed through the USB bus to the main control machine. The host will send a command to the collection board to Whether or not save the data. If data needs to be saved, the data will be stored in a large capacity of SRAM by the system logic circuit; if the data is not necessary to save, then the data in the buffer will be later covered by the data.

2.2. Collection System Characteristics

Traditional radar data acquisition is usually used in the " open a window to collect ". This acquisition method relies on the tracking algorithm, if the window is too large, it will gather a lot of useless information, and can cause resource waste; if the window is too small, it will lost some useful information, bring difficulty to the recognition of the target. In addition, if the target is larger and the tracking algorithm can't make good prediction, it will not be possible to collect the target information in the next week, so that the target data may be lost.

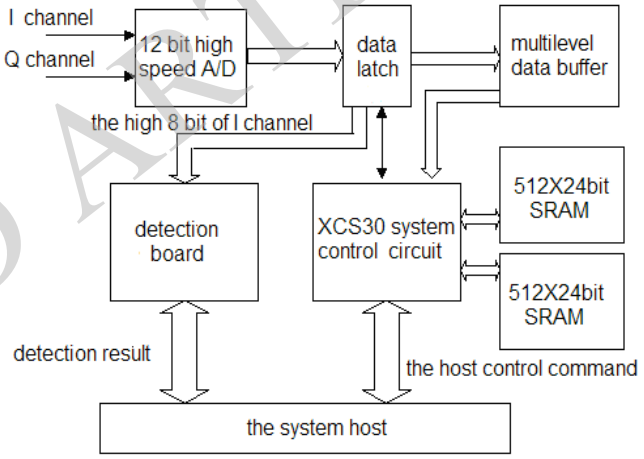

Fig. (1). schematic diagram of dual channel radar data acquisition system.

The collection system presents a scheme of "0 circle scan acquisition". The so-called "0 circle scan acquisition" is the combination of the rough acquisition of the target detection and the precise acquisition of the feature extraction, the accurate acquisition on the target echo was not discovered until the target after scanning start next week, but all the time. The "0 circle scanning acquisition" scheme has solved the real-time performance of the radar target acquisition, and has overcome the phenomenon of the target information loss in the traditional radar target data acquisition.

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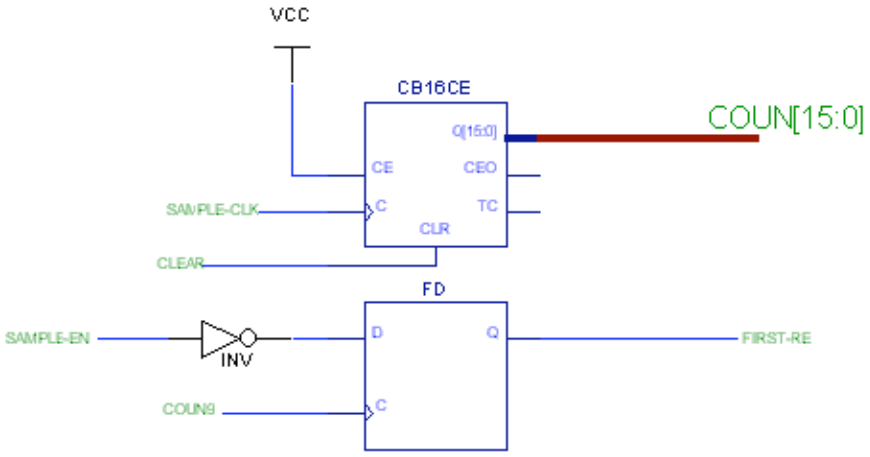

Fig. (2). Schematic diagram of FIFO read and write control circuit.

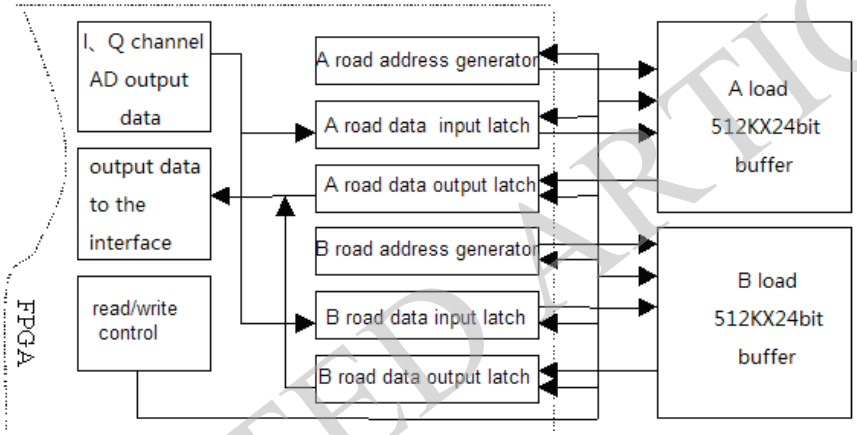

Fig. (3). Schematic diagram of the large capacity buffer.

3. SYSTEM LOGIC CONTROL CIRCUIT DESIGN

3.1. Multi-Level Data Buffer Control

In order to ensure the acquisition board when it receives the test results, the batch of data still in the buffer zone, the system design four level data buffer[2], in the circuit design, each level of data output control signal with the next level of input control signals use the same control line, so the hardware obstacle free to read and write timing confusion and possible data loss. Before starting the data acquisition, the control circuit will automatically reset the address of the FIFO [3].

System debugging, set up the wait time is 256 bytes, circuit as shown in Fig. (**2**), 16 bit counter in each began collecting will reset, when the counter counts up to 256 bytes, the ninth data line of the counter is changed from low to high, The input end of the trigger is acquisition enable signal after the reverse, after collecting 256 points, the first level FIFO data start to output. The second, third and the fourth trigger signal is the tenth, eleventh and twelfth root data output line respectively. The output of the last stage is equivalent to the delay of the 1K byte.

3.2. High Speed and Large Capacity SRAM Control

The memory of this system is AS7C4096. In the circuit, mainly design the two memory (a, b), constitute "toggle switch" type structure[4] provided read or write signals (re, we) by the FPGA the advantage of this structure is that a group of memory is written in the same time, the host read operation to another set of memory.

the benefits of this structure is to a set of memory write operation, host also a group memory read operation, so that the collector can collect data and transmit data at the same time, the system can output data at the speed of fast as far as possible, to meet the requirements of acquisition for a long time[5].

Since I, Q two channel AD conversion has 24 bit data output, Each road need to use 3 piece AS7C4096 chips with 512K * 24bit high speed and large capacity buffer. The control signal of 3 piece AS7C4096 chips of each road is given by FPGA. In circuit design, due to the limitation of the I/O pin resources, a piece CPLD chip is added to produce the address signal for AS7C4096. A set of address lines are shared with 3 pieces of memory in the same road, and the data line is connected in bit extension manner but the data line is separated

Using FPGA and CPLD to control system logic and address generation, greatly reduced the difficulty of data acquisition system address and control signal timing relationship and its components principle block diagram is shown in Fig. (**3**).

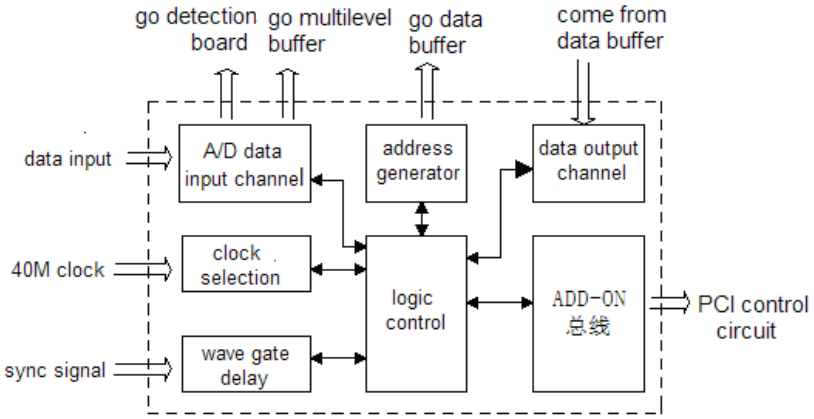

Fig. (4). system logic control function chart.

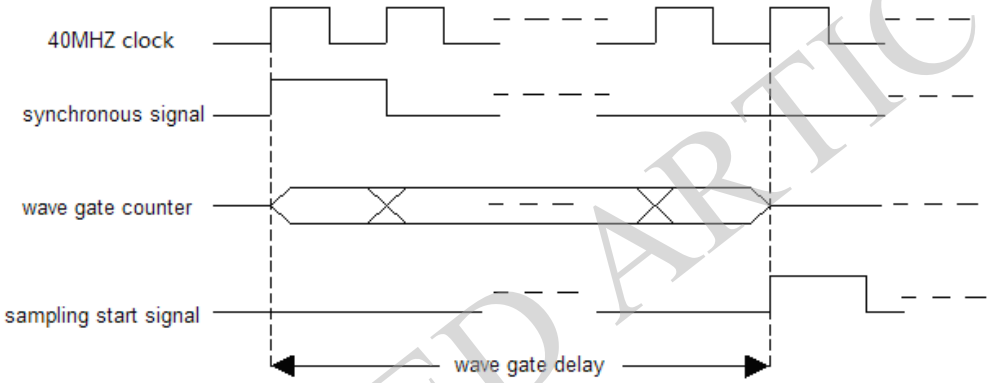

Fig. (5). Digital gate timing diagram.

3.3 Automatic Acquisition Control Circuit Design

Multi target automatic acquisition system control circuit mainly includes data acquisition timing, system logic relation and interface circuit timing. All logic relations of entire system are completed by a piece Spartan XCS30 and a piece CPLD XC95108 of XILINX company. The function of the control circuit is shown in Fig. (**4**).

3.3.1. Clock Generation Circuit

Because the collector has multiple sampling rate, so the clock circuit is designed to count and divide frequency on the 40MHz clock, for different target can choose different sampling clock, realizes in a specific way is through the host command is issued, which contains four clock select bit. Four clock select line control an alternative MUX, at the same time to ensure that the collector can collect other signals without the external synchronization signal, the internal synchronization signal of 100Hz-5000Hz is obtained by dividing the frequency of the clock, the same logic circuits selects the output.

3.3.2. Data Selection and Gate Delay Circuit

After the detection system detects the target, through the host issued

Orders may be issued by the host, to generate a control signal to control the wave gate [6], logic circuit will select the needed data from multiple buffer according to the wave gate information. If the detection and collection work separately, when the acquisition board is interval sampling, sampling circuit only work in the wave gate, so must enable acquisition gate can accurately at the target, in order to accurately collect target data. The collector is the use of the digital Wave gate method, the specific method is to use the 40MHz clock to design the delay counter, according to the target distance calculated how much delay, start delay counter after the synchronization signal is triggered, after precise delay restart collector to collect data. Its working timing is shown in Fig. (**5**).

3.3.3. Repeat Collection and Control

To radar echo signal acquisition of repeating the cycle is a requirement of radar target recognition for acquisition system.

In order to accumulate more information in time domain, frequency domain and target shape and attitude, more information is accumulated on the attitude to improve the accuracy of the recognition system, each cycle echoes of the target is required to collect, working process is shown in Fig. (**6**).

The radar echo signal is composed of two parts: the synchronous signal and the target echo signal, usually radar data acquisition system to collect generally target echo signal,

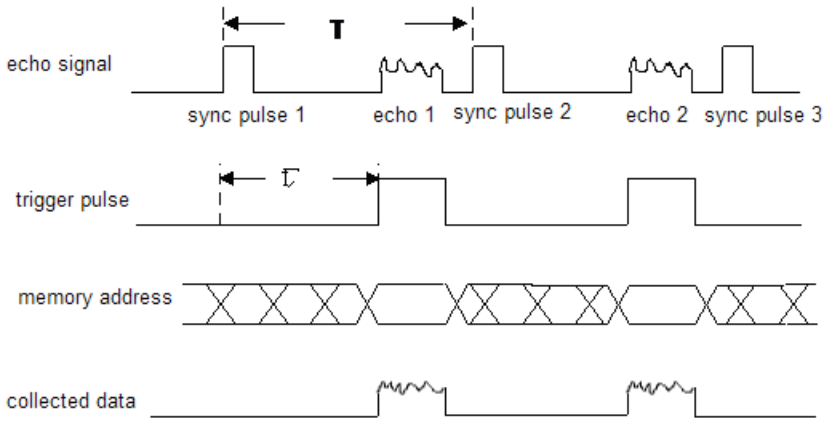

Fig. (6). Repeat acquisition of radar echo.

Therefore, a control circuit is designed to generate a delay signal that is equivalent to a radar synchronization pulse, this signal triggered acquisition target echo signal. the acquisition time is controlled by the length counter, after collecting the echo signal of the cycle, waiting for acquisition of the next cycle, repeat this, until the number of repeat counter to achieve the set value, and end data acquisition process.

3.3.4. Multiple Target Tracking and Acquisition

In the circuit implementation, the first in the FPGA to open up the 1K storage space, used to store the target information.

Usually sampling circuit track and collect a target, when received the command that the host machine start another target acquisition, sampling circuit will automatically track and collect another target.

CONCLUSION

In this paper the logic control circuit of radar data acquisition system is designed by using FPGA and CPLD chip, "0-circle scanning acquisition scheme of the data acquisition system is brought forward from the hardware solves the real-time of radar data acquisition, overcomes the phenomenon of target information loss existing in the traditional radar target data acquisition, the acquisition system has been successfully application in a certain type of radar target recognition prototype, and has strong application value.

CONFLICT OF INTEREST

The authors confirm that this article content has no conflict of interest.

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